[[1]](#footnote-1)

CmpE 124 Lab 2: Signal Generator Test

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*Abstract*—Lab two’s report is a breakdown and analysis of the purpose for lab two which was to create a clock- counter circuit that was to act as a signal generator for testing and observing how NAND, NOR and EOR gates function.

# INTRODUCTION

The basic function and purpose (importance) of the design will be discussed here. The clock-counter circuit is a 4 bit binary counter that counts from zero till binary number 15. By using the 74LS163 as the counter and a 10MHz crystal the circuit can be used as a signal-generator allowing additional testing with 74LS00, 74LS02, and 74LS86 gates. The gate characteristics can be then observed by using the oscilloscope.

# Design methodology

## Parts List

* 1 x 10Mhz Crystal
* 1x 74LS00
* 1x 74LS02
* 1x 74LS86
* 2x 74LS04
* 1x 74LS163

## Truth Tables

|  |  |  |
| --- | --- | --- |
| Truth Table For 74LS00 NAND Gate | | |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
|  |  |  |
| Truth Table For 74LS02 NOR Gate | | |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
|  |  |  |
| Truth Table For 74LS86 EOR Gate | | |
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## Original and Derived Equations

Equation for 74LS00 NAND Gate

Equation for 74LS02 NOR Gate

Equation for 74LS86 EOR Gate

## Schematics

See attached schematic [2] under appendices and reference. The schematic shows three gate outputs labeled as 74LSXX Output and shows the standard output of the 74LS163 labelled as Q1, Q2, Q3, Q4. The clock is an input to the CLK pin, while the RCO is labeled as an output. The label Fin1 is a branch label that provides appropriate signals to LOAD, P, T, while the CLR pin is controlled by a binary switch to allow manual reset during simulation.

# testing procedures

1. Assemble Circuit as soon in figure [2] under section VI.
2. Connect Oscilloscope probe to each output Q# and observe.
3. Connect outputs Q0 and Q1 to each gate:
4. 74LS00
5. 74LS02
6. 74LS86
7. Connect Oscilloscope probe to output of current gate being tests.
8. Compare results with simulation results

Figure [3] shows schematic [2] simulation result. The Clock being reference waveform is on top, under it the RCO which shows reset at the end of each clock period. The outputs Q1, Q2, Q3, and Q4 are grouped and are shown as 16bit hexadecimal. The three gate outputs are shown to easily observe the outputs. This will be compared to the results gathered in step four to see if the provided gates are close to ideal functionality.

# testing results

Under section VI picture [1-4] provide oscilloscope readings and observations. Picture [1] bottom waveform is the 74LS00 output with the clock and the RCO as reference under the clock as the reference waveform. Picture [2] bottom waveform shows the output of the 74LS86 and follows picture ones reference output. Picture [3] shows L74LS02 output below the clock and RCO. Picture [4]\shows the output of all four outputs from the 74LS163 with reference to the clock, the first half of the clock cycle is on the positive x-axis and the negative x-axis shows the second half of the clock cycle.

Comparing pictures 1, 2, 3 to figure [3] the waveforms within one clock period match for all three gates. Each gate has eight transitions from the either high to low or vice versa. Also each gate follows the provided expressions and table, for example the 74LS02 is only High when the counter is at binary zero, four, eight, and twelve which is when the LSB and succeeding bit are both 0. This shows that the tables and waveforms match the expression for each gate.

# Conclusion

By creating a binary counter the three gates were observed on the oscilloscope and compared to the simulations. The waveforms were near identical apart from some variation as a component does not function ideally. Each rising edge form the clock is a stage, during the rising edge the output are either HIGH or LOW respective to the binary count. At different stages each of the three gates were triggered as the relating expression was true.

For observations of the each clock period which is fifteen cycles from HIGH and LOW a reference was needed to observe when binary the count had reset at binary zero. The reference was the Ripple Carry Output which is the triggered once a carry bit is generated. This would be at fifteen when the count needs to reset which is why a spike is caused in the RCO. Hence to look at one full clock period the RCO was chosen as reference as looking from RCO spike to the next would show the full count to fifteen.

By comparing and observing the gates through an oscilloscope the functionality and much more clear. As the table do not clearly tell how the gate works but can only tell when the gate will work. However some questions remain unanswered such as what is the actual use of such gates and how they are implementing in circuitry. Overall the execution of the lab was success as the results match to the expected.

# appendices and references

[1] Özemek, Haluk. (2014, Aug 14). 124\_Labs [Online]. Available: https://sjsu.instructure.com/courses/1142847/files

Schematic [2]: Full page print out of simulation circuit.

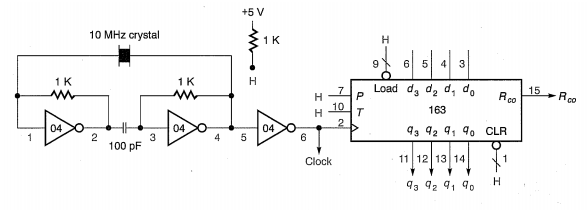
Figure [3]: Taken from [1]

Figure [4]: Full page print out of simulation waveforms.

Picture [1-4]: Full page print outs of oscilloscope waveforms.

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